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Discontinuous Quasi-2-Level Modulation for MV applications

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Abstract

The concept of Quasi-2-Level (Q2L) modulation is a potential alternative to series-connected semiconductors with bulky passive snubber as well as complex multilevel converters in medium voltage (MV) domain. The key idea is to operate a multilevel converter in a 2–level manner with a brief delay between switching the series-connected semiconductors. This approach allows to ensure equal voltage distribution between the switches and to minimize the system size by utilizing smaller capacitors. On the other hand, the number of series-connected switches in Q2L converters limits the maximum switching frequency. This study shows the advantages of discontinuous Q2L (DQ2L) modulation to increase these limits. The experimental results demonstrate that the DQ2L increases the switching frequency limitations. Furthermore, the capacitor current rms is reduced by 37% when the DQ2L is employed.

1 Introduction

Medium voltage (MV) DC grid configuration is gaining a significant role in the distribution or sub-transmission networks related to the emerging number of DC-based loads, including data centers, transportation systems, and fast charging stations for electric vehicles [1]. Fig 1 shows an example of the MVDC grid infrastructure with several possible DC and AC loads. Despite the advantages, the MVAC grid remains dominant and an interface between the existing MVAC and the emerging MVDC grids is essential [2]. The interface converter must be synchronized with the MVAC grid and capable of providing the bi-directional power flow. This way, it becomes possible to establish grid support in both directions and provide better flexibility.

One of the biggest challenges for the MV applications is designing a highly efficient power converter with a high power density that can be achieved by utilizing fast and efficient semiconductors, e.g., Silicon Carbide (SiC). Since the maximum voltage of modern SiCs is limited, a multilevel converter topology is required for direct connection to the MVDC grid.

Quasi-2-Level modulation (Q2L) of multilevel converters draws remarkable portion of interest from the academia and the industry. It allows to increase the potential voltage range of a converter by providing the means to facilitate equal

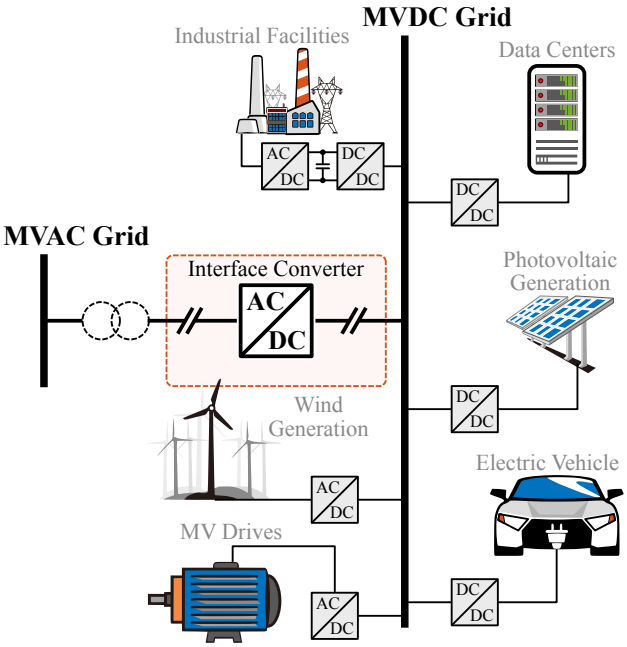


Fig. 1: Example of MVDC grid infrastricture with the interface converter combining the MVDC and MVAC grids.

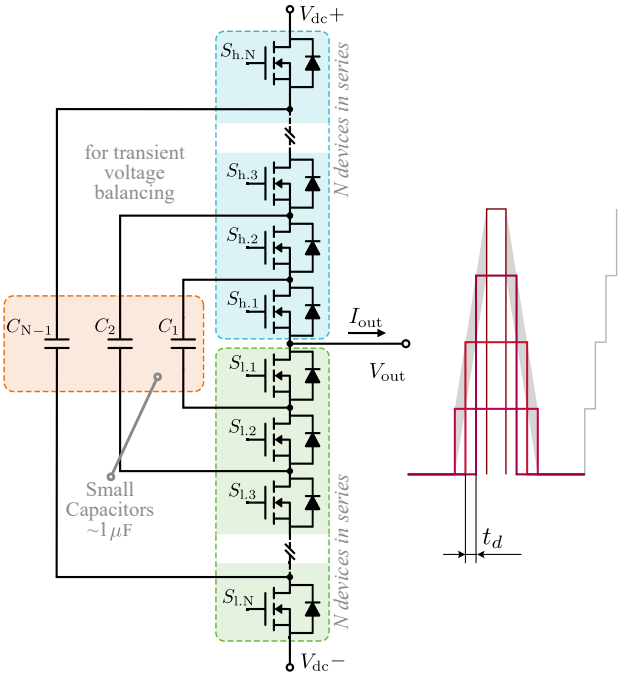


Fig. 2: N-step Q2L converter leg, utilizing small flying capacitors. The capacitors are only used to provide the intermediate voltage to the semiconductors during the switching transition.

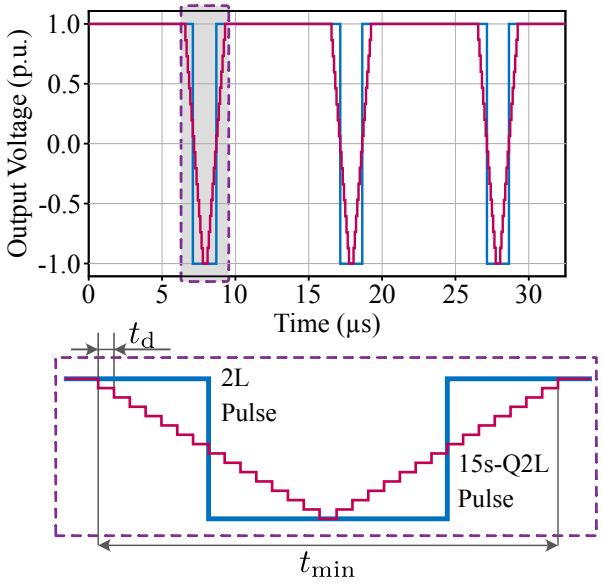


Fig. 3: Example of the duty cycle limitation in Q2L modulation.

voltage sharing between the series connected semiconductor switches without any additional circuitry. Furthermore, the volume of the components inherent to a particular multilevel topology can be reduced significantly. Fig. 2 demonstrates an example of N-step Q2L Flying Capacitor (FC) converter. The capacitor units in Q2L FC are required to create the intermediate voltage reference during short transients, therefore their total volume is several orders of magnitude lower than that of the full-scale multilvel converter [3]–[8].

The idea behind the Q2L modulation is to switch the devices sequentially, letting each device to fully change the state prior switching the next one. In other words, during the turn-on, the first device in the sequence needs to change its state and to be fully on before commutating the next device in the sequence. However, due to the finite switching time of the semiconductors, the holding time of each device cannot be infinitely small. As a result, increasing the number of steps limits the maximum duty cycle at which the output waveform becomes trigonal, as shown in Fig. 3. Due to this limitation, multistep Q2L converters with high number of semiconductors are very limited in terms of the switching frequency.

This paper investigates Discontinuous Quasi-2-Level (DQ2L) modulation as a remedy to the duty cycle and the switching frequency limitations. Furthermore, applying DQ2L modulation curtails the current ripple of the capacitors, significantly reducing the capacitance requirement and therefore the total volume of the capacitor blocks. The conducted study is verified both analytically and by experiments.

2 Multistep Q2L FC for MV grids.

Fig. 4 shows possible configurations of a single Q2L FC converter leg, depending on the voltage class of Silicon Carbide (SiC) MOSFETs, suitable for the connection to 10 kV MVAC grid. As an example, the Q2L FC based on 1.2 kV semiconductors requires 42 switches and 21 capacitor units per leg. Alternatively, selecting 3.3 kV devices reduces these numbers to 16 SiC MOSFETs and 7 capacitor blocks.

It has been demonstrated that Q2L FC with increased number of steps significantly limits the maximum switching frequency and modulation index of the converter [3]. According to Fig. 5, 15s-Q2L with 200 ns delay time can achieve less than 18 kHz switching frequency. Reducing the delay time to 100 ns increases the possible switching frequency to 35 kHz. The switching frequency can be further increased, by reducing the modulation index. However such approach will cause additional stress on the devices due to increased dc-link voltage.

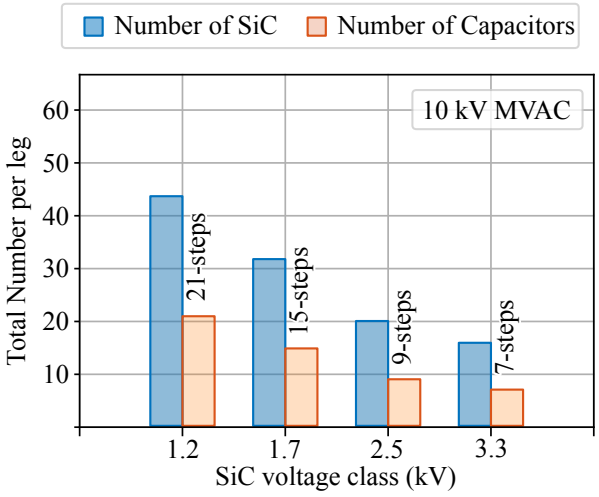


Fig. 4: Total number of devices per leg required for 10 kV MVAC. The blue bar represents the number of semiconductors, whereas the orange bar shows the number of capacitor blocks per leg.

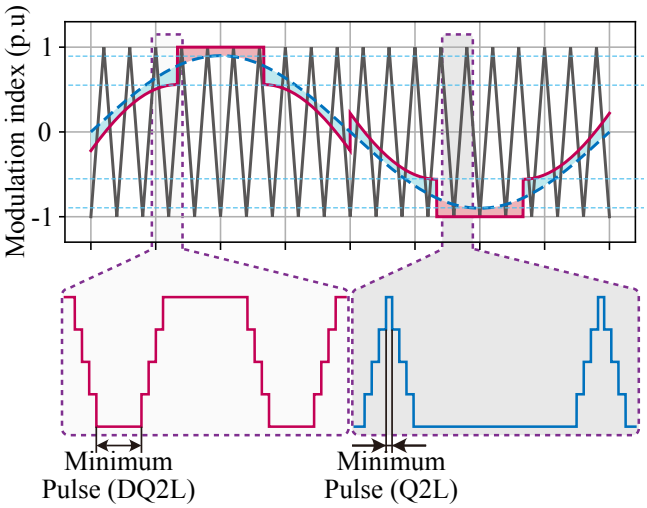


Fig. 6: DQ2L and Q2L modulation waveforms comparison with corresponding PWM pulses at the highest duty cycle. Q2L is shown as the dashed blue line, whereas DQ2L is represented with the solid magenta line.

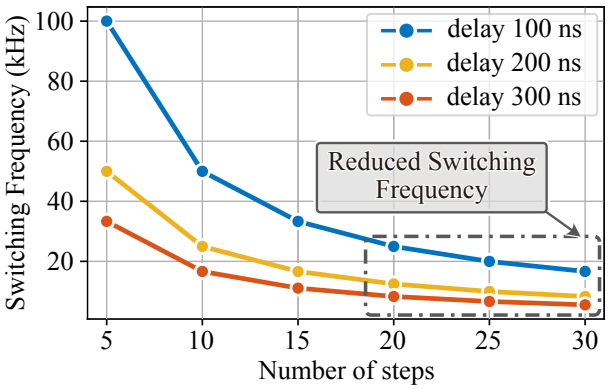


Fig. 5: Maximum switching frequency limitation of Q2L modulation for various delay times and different number of steps.

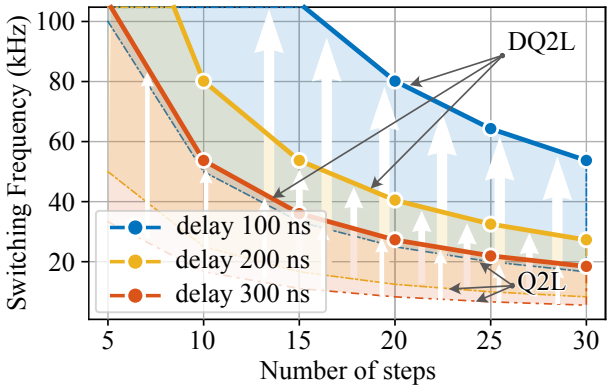


Fig. 7: Theoretical limitation of the DQ2L PWM (solid lines) compared to Q2L PWM (dashed thin lines) for different delay times.

3 Discontinuous Q2L Modulation

Since the increased number of steps in Q2L modulation limits maximum allowable pulse width, the maximum switching frequency and the modulation index are also limited. DQ2L modulation adds the third harmonic and its indices to the ideal sine-wave reference. The amplitude of the final reference is limited by the value of $M\sin(\pi/3) = 0.86M$, thus the maximum modulation index is increased by 15%. The waveform is obtained by adding a calculated offset to a pure sine-wave [9].

Fig. 6 demonstrates the DQ2L reference waveform and resulted PWM for the unity Power Factor (PF) scenario. Conventional Q2L PWM is shown as the dashed blue line, whereas DQ2L PWM is shown as the solid magenta line. It can be observed that the waveform is clamped to the rail at the points of sine-wave amplitudes. These region do not have any PWM switching. Furthermore, the area with the minimum pulse width is limited to $\pm\sin\left(\frac{\pi}{3}\right)$. Therefore, for the DQ2L, the whole area between the clamping states is pushed down by the added offset, yielding the maximum value of the modulation index:

$$M_{\mathrm{dq2l}} = M \cdot \sin^2\left(\frac{\pi}{3}\right) \tag{1}$$

where M_{dq2l} is the modulation of the DQ2L.

The lower part of the figure shows the resulting PWM of the maximum duty cycle for DQ2L (left) and Q2L (right), where the minimum pulse of the DQ2L PWM is increased significantly compared to

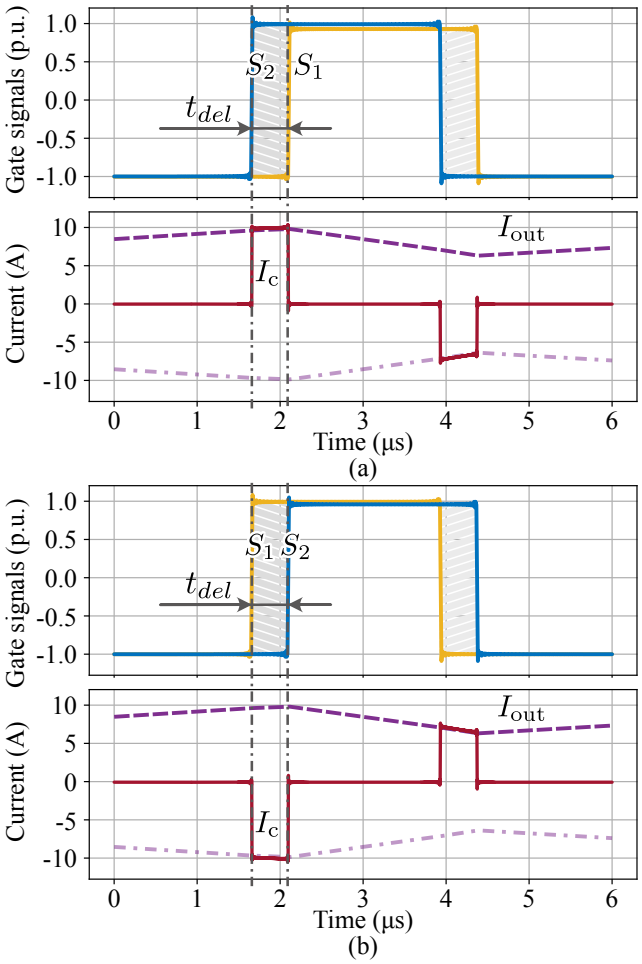


Fig. 8: Capacitor current direction depending on the switching sequence: (a) S_2 turns-on before S_1, and (b) S_1 turns-on before S_2.

the minimum pulse of the Q2L PWM. The minimum pulse is increased compared to the Q2L modulation. As a result, the multistep Q2L converter can reach higher switching frequencies with the DQ2L, as shown in Fig. 7. As an example, the switching frequency of 15-step converter configuration with 200 ns delay time is increased from 18 kHz to 56 kHz.

4 Capacitor Current in DQ2L

The capacitor current of Q2L FC flows through the capacitor twice per switching period during the delay times at both turn-on and turn-off events. The capacitor current changes the direction after each pulse in order to maintain its voltage around the specified level. Fig. 8 demonstrates a single switching period with the capacitor current of Q2L FC. The current only flows during the holding time between two adjacent switches (in this example S_1 and S_2). Furthermore, when S_2 is turned-on first,

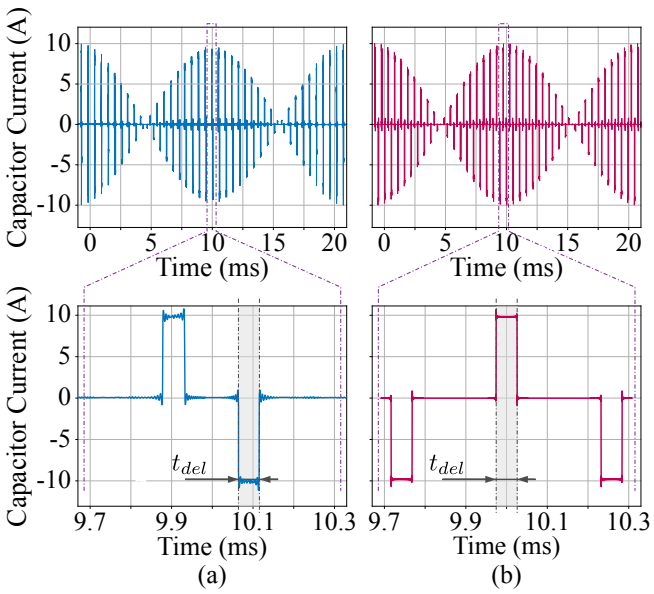


Fig. 9: Plotted time-domain waveform of the calculated capacitor current. Switching frequency - 2 kHz, delay time - 500 μs: (a) waveform based on full equation, and (b) waveform based on the simplified equation.

as shown in Fig. 8 (a), the current flows through the capacitor and the direction of the current is positive. As soon as the second switch S_1 turns-on, the capacitor current ceases. Alternatively, turning-off S_2 first invokes the current flow out of the capacitor to the load. Fig. 8 (b) demonstrates the opposite switching sequence of Q2L FC where the inner semiconductor S_1 is turned-on prior the outer device S_2. In this case, the current is negative at the turn-on and positive at the turn-off.
Analytically, the current of each capacitor can be calculated as a switching function S with the duty cycle $d = 4t_{\mathrm{del}}/T_{\mathrm{s}}$ multiplied with the load current:

$$
\begin{aligned}
I_{\mathrm{c.q2l}} = I_p \sin(\omega_{\mathrm{o}}) \times \frac{4}{\pi} \sum_{m=1}^{\infty} \sin^2\left(m\frac{\pi}{2}\right) \times \sin(m\omega_{\mathrm{c}}) \\
\times \left[dV_{\mathrm{dc}} \cos(\omega_{\mathrm{o}}) + \frac{8V_{\mathrm{dc}}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0\left(m\frac{\pi}{2}M\right) \right. \\
\times \cos\left(\frac{m\pi}{2}\left(1+\frac{d}{2}\right)\right) \times \cos(m\omega_{\mathrm{c}}) \\
+ \frac{8V_{\mathrm{dc}}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} J_n\left(m\frac{\pi}{2}M\right) \\
\left. \times \cos\left(\frac{\pi(m+n)}{2}\left(1+\frac{d}{2}\right)\right) \times \cos(m\omega_{\mathrm{c}} + n\omega_{\mathrm{o}}) \right]
\end{aligned}
\tag{2}
$$

where I_{pk} is the peak value of the output current,

ω_o and ω_c are the fundamental and PWM radial frequencies and m is the switching frequency harmonic index.

The equation above is overcomplicated by the fact that the pulse current of the capacitor with the time t_{del} is placed at the beginning and at the end of the PWM pulse. For the rms calculation, the placement of the pulses within the switching period does not play any role. The number of switching instances over the fundamental period and the width of each pulse are the only factors determining the rms. Like this, (2) can be then simplified to:

$$I_{c.q2l} = I_{pk} \sin(\omega_o) \cdot \sum_{m=1}^{\infty} \frac{1}{m\pi} \sin(m\pi d) \times (1 - \cos(m\pi)) \times \cos(m\omega_c) \quad (3)$$

The plotted time-domain waveforms of the flying capacitor current in (2) and (3) are demonstrated in Fig. 9 (a) and 9 (b), respectively. For simple representation, the switching frequency in is 2 kHz and the delay time is 500 μs. To calculate the rms of the capacitor current, the square of (3) has to be integrated within the limits of the switching period T_s:

$$I_{rms} = \sqrt{\frac{1}{T_s} \cdot \int_0^{T_s} I^2(t) dt} \quad (4)$$

Rearranging (3) and applying it to (4) yields the relation for evaluating the rms of the capacitor current based on the delay ratio between the delay time and the switching period:

$$I_{q2l.rms} = I_{pk} \sqrt{\frac{t_{del}}{T_s}} \quad (5)$$

The instant value of the capacitor current during the delay time equals the instant load current, but due to a very short delay time, the current rms is relatively low as compared to the load current amplitude. Moreover, implementing the Q2L modulation with as shortest as possible delay time, will not only minimize the capacitor current rms, but will also reduce the required capacitance value as well as the volume of the whole capacitor block.

During the Discontinuous modulation stage, when the converter leg is being clamped to the dc-rail the current flows to the load through the opened switches, avoiding the flying capacitors. The capacitor current under the discontinuous

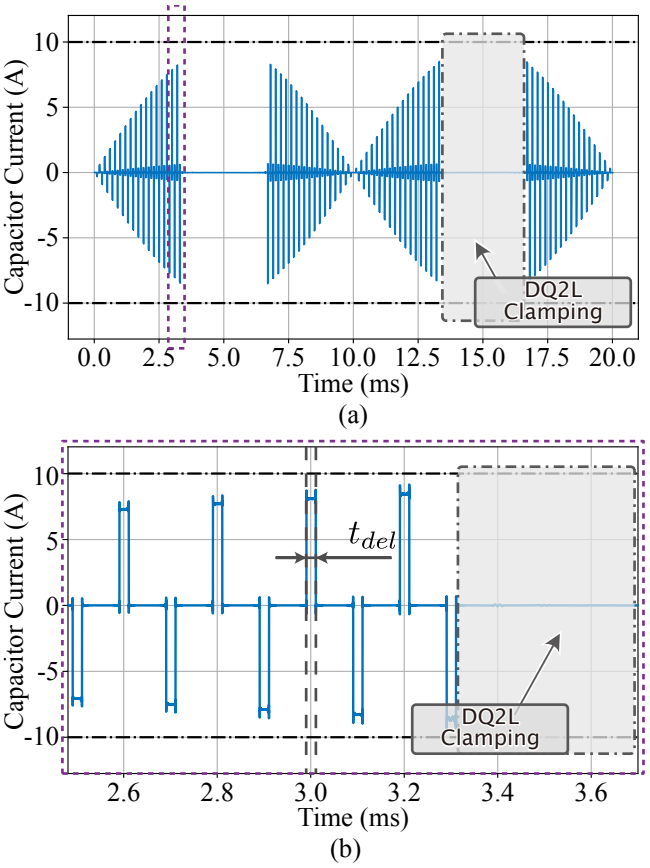


Fig. 10: Plotted time-domain waveform of the calculated capacitor current in DQ2L FC. Switching frequency - 2 kHz, delay time - 500 μs: (a) fundamental period view, and (b) switching period view.

modulation is expressed as:

$$I_{c.dq2l} = 2 \cdot I_{pk} \sin(\omega_o t) \times \sum_{m=1}^{\infty} \left[\frac{2}{3} + \frac{1}{m\pi} \cdot \sin\left(\frac{2\pi}{3} m\right) \times \cos(2m\omega_o t) \right] \times [\sin(m\pi d)(1 - \cos(m\pi))] \times \cos(m\omega_c t) \quad (6)$$

Fig. 10 shows the plotted expression (6) with the clamped discontinuous area highlighed as the gray box.

Since this maximum current does not flow through the capacitors anymore, the resulting also rms decreases. The rms current of DQ2L modulation depends on the delay time, switching frequency and peak output current:

$$I_{dq2l.rms} = \left[\sqrt{\frac{2}{3} - \frac{\sin\left(\frac{2}{3}\pi\right)}{\pi}} \right] \cdot I_{PK} \sqrt{t_{del} \cdot f_{sw}} \quad (7)$$

where the expression in square brackets represents

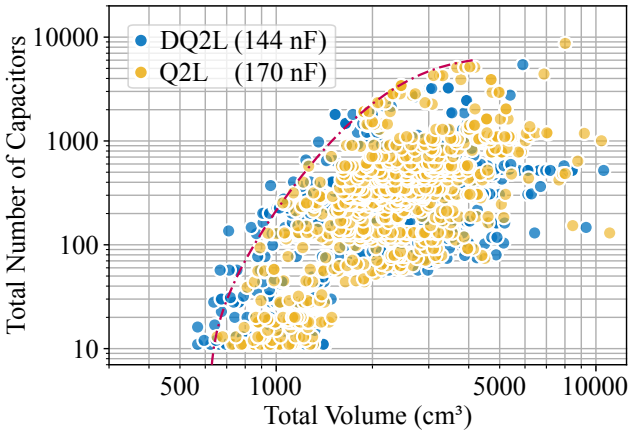


Fig. 11: Total number and volume of capacitors required for 10 kVAC 7s-Q2L and 7s-DQ2L converter.

the contribution of the discontinuous operation with the reduction factor of 0.623.

Therefore, the rms of the capacitor current under the DQ2L modulation is 37% less than that of the continuous Q2L. Moreover, since the instant value of the capacitor current at the clamping point equals $I_{\mathrm{pk}} \sin(2\pi/3)$, the required capacitance is decreased by 15% compared to the Q2L FC.

Fig. 11 shows the volume and device number requirement for 7 capacitor units (10 kV MVAC) with DQ2L and Q2L modulations. Fig. 11 considers 180 A peak current, 5% voltage ripple and 200 ns delay time. The required capacitance is calculated according to [3], [5]. To estimate the total volume and the number of capacitors, a database with over 500 capacitors has been evaluated. For each entry of the database the number of series connected capacitors to comply with the designated voltage level has been calculated first. Further, to satisfy the capacitance requirement, the number of parallel devices has been evaluated. Afterwards, the volume of a single unit has been multiplied with the required number of series and parallel connections. As can be observed, the total volume of capacitors for DQ2L modulation is reduced compared to that of the Q2L modulation. In this example, the volume has been reduced by approximately 100 cm^3.

5 Experimental Results

The experiments have been conducted on a 3-step Q2L flying capacitor full-bridge converter prototype shown in Fig. 12. The prototype uses SCT90N650GT SiC MOSFETs from ST semiconductors. The parameters of the experimental setup are given in Table 1.

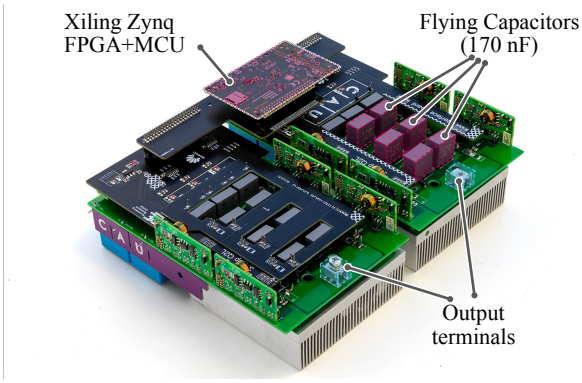


Fig. 12: 3s-Q2L flying capacitor full-bridge converter prototype used for the experiments.

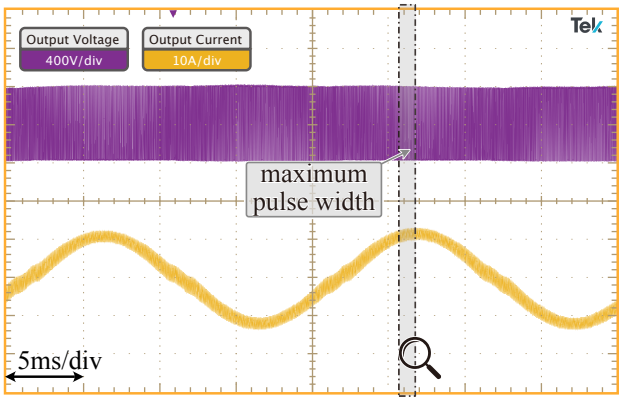
Switching frequency	f_{sw}	50 kHz
Fundamental frequency	f_{o}	50 Hz
DC-link voltage	V_{dc}	800 V
Flying capacitors	C_1–C_3	170 nF
Filter inductance	L_{out}	0.5 mH
Load resistance	R_{out}	25 Ω

Tab. 1: Experimental parameters

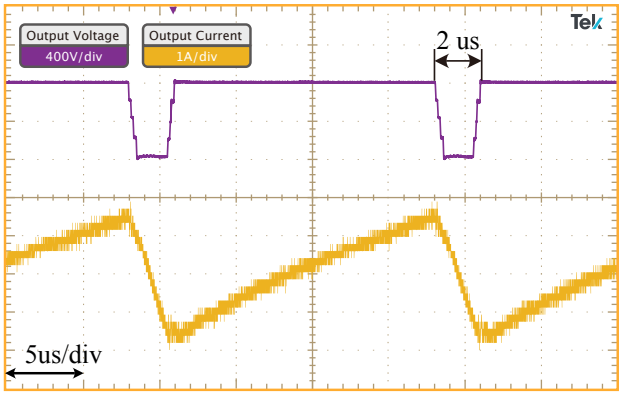
The experimental results of the Q2L modulation are demonstrated in Fig. 13. Fig. 13 (a) provides the fundamental frequency view with 5 ms/div horizontal scale. The area with the maximum pulse width occurs around the current amplitude. It is highlighted with a grey box. The magnified view on the Q2L switching region is demonstrated in Fig. 13 (b). The pulse with maximum width is around 2 μs. As can be observed, the rising and falling edges of the Q2L modulation with 150 ns delay/step already occupy the half of this time range. Increasing the number of steps will affect the maximum switching frequency and the modulation index of the converter.

The experimental results of the DQ2L modulation are shown in Fig. 14 (a) with the fundamental frequency view (5 ms/div) and Fig. 14 (b) showing detailed switching instance at 5 μs/div. Here the pulse with the maximum width occurs before the current reaches its amplitude, since the switching halts due to the discontinuous operation. Therefore, the it is considerably wider that that of the Q2L modulation. From Fig. 14 (b) it can be seen that the maximum width pulse is 7 μs, that is 3 times longer than in the case of the Q2L modulation.

Fig. 15 demonstrates the capacitor current under DQ2L modulation. The current profile matches with the plotted waveform (6) in Fig. 10. Clearly, the

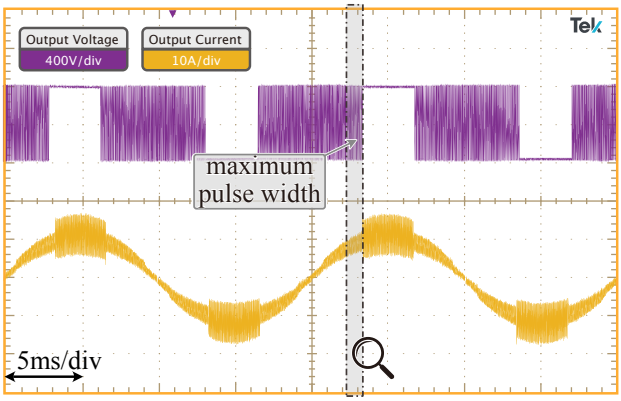


(a)

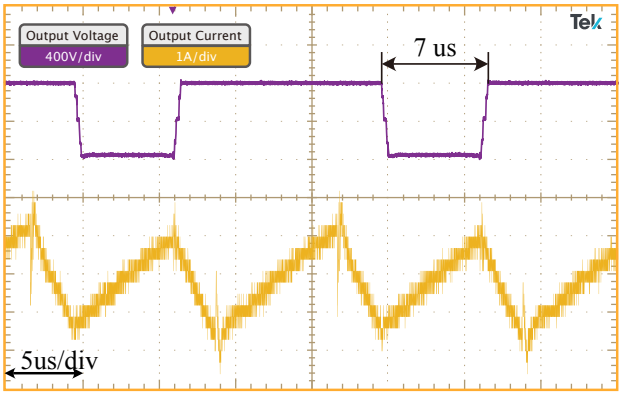


(b)

Fig. 13: Experimental results of the 3s-Q2L modulation: (a) fundamental frequency view, and (b) switching frequency view.



(a)



(b)

Fig. 14: Experimental results of the 3s-DQ2L modulation: (a) fundamental frequency view, and (b) switching frequency view.

current ripple reduces to zero as the converter leg proceeds into the discontinuous operation mode. This curtails the stress on the flying capacitor and reduces the rms of the total current.

6 Conclusions

This paper investigates the advantages of Discontinuous Quasi-2-Level (DQ2L) modulation for medium-voltage (MV) converters utilizing Quasi-2-Level (Q2L) modulation concept. Although Q2L modulation can be used to provide equal voltage sharing between multiple series-connected semiconductors, the required delay between each step can significantly reduce the switching frequency capability and the maximum modulation index of the converter.

By using the DQ2L modulation in MV converters it is possible to increase the switching frequency more than 3 times compared to the conventional Q2L method. As a result, the size of dc-link capacitors and line filters can be reduced. Furthermore, the maximum modulation index is not limited by the number of series connected

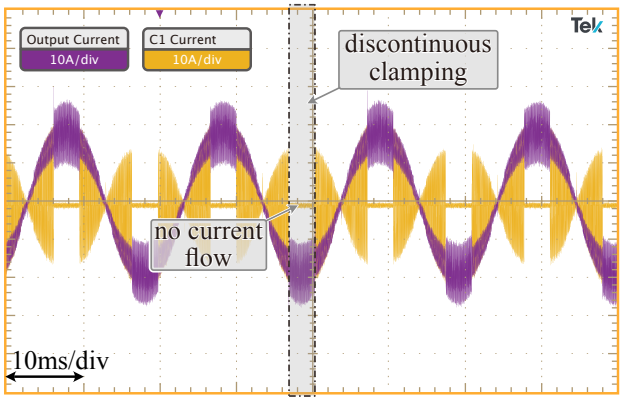


Fig. 15: Experimental results: output and flying capacitor currents under the DQ2L modulation of 3s-Q2L FC full-bridge.

semiconductors and the delay time. Hence, the dc-link voltage can be regulated in the higher range. Another major advantage of adopting discontinuous Q2L modulation is that the total capacitors volume can be reduced since there is no current flow during the discontinuous stage. This reduces the rms by approximately 37%.

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